IDEC Chip Design Contest

Area and Power-Efficient PLL Design in 30 nm FD SOI Technology: Compactness, Low Power, and Enhanced Locking Range

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▪ MOTIVATION

- Conventional ring and LC VCOs either consume excessive power or occupy large die areas, driving the search for efficient architectures.
- Modern systems demand PLLs that combine broad tuning ranges, minimal footprint, and low energy usage in a single integrated block.
- D-latch-based VCO unites these goals, delivering precise frequency control and ultra-low power consumption across operating conditions.

▪ Features of the D-Latch-Based Voltage Controlled Oscillator (VCO) Architecture

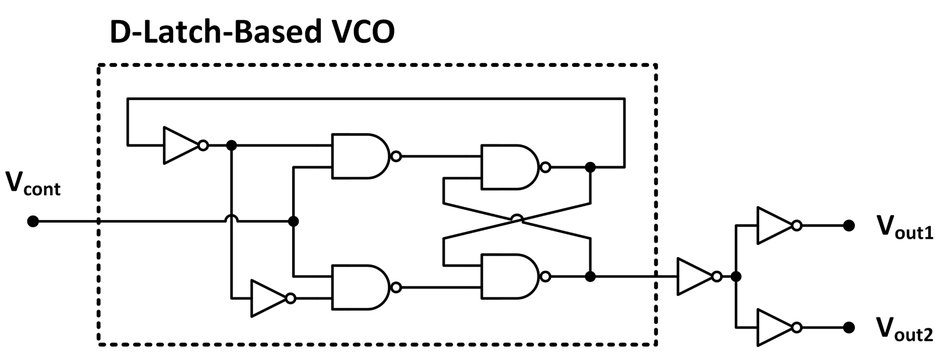
- A D-latch feedback loop ensures stable oscillations and accurate frequency control under varying conditions.
- The latch's intrinsic regenerative latching eliminates extra buffers, reducing both silicon area and power draw.
- The low-pass filter's control voltage directly tunes oscillation rate across a wide frequency span.
- Streamlined topology minimizes circuit complexity and die size for rapid prototyping and high-volume fabrication.
- Single-chip integration replaces bulky LC or ring designs, delivering a compact footprint with proven reliability.
- Minimizes oscillator startup time through the D-latch's regenerative feedback, ensuring reliable initial oscillation across varying operating conditions.

▪ Phase Locked Loop (PLL) Architecture

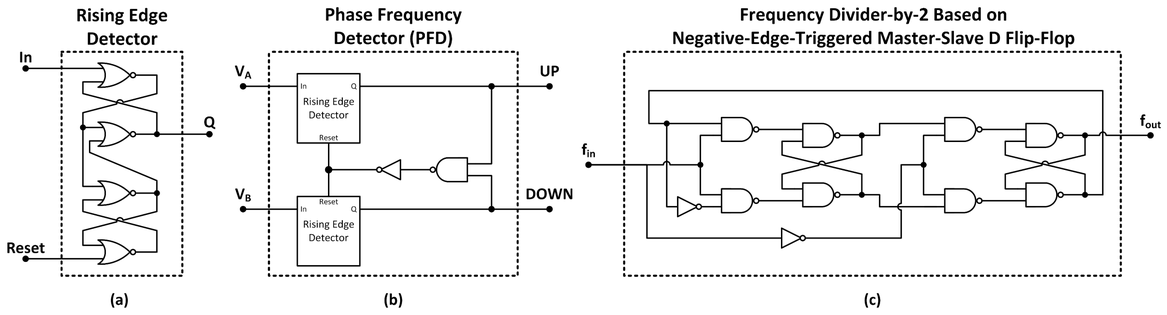
- The PLL comprises a PFD, Charge Pump, Low-Pass Filter, frequency dividers, and a D-latch-based VCO.
- The PFD (two NOR-based positive edge detectors) and dedicated inverters drive the Charge Pump for accurate phase/frequency control.
- The Charge Pump uses balanced PMOS/NMOS current sources, while a transmission-gate resistor and capacitor in the Low-Pass Filter stabilize the VCO control voltage.
- Frequency division is handled by negative edge-triggered D flip-flops for precise division ratios.
- The D-latch-based VCO (without extra ring buffers) provides stable oscillations, reducing power and ensuring a broad locking range

▪ Performance Highlights and Conclusion

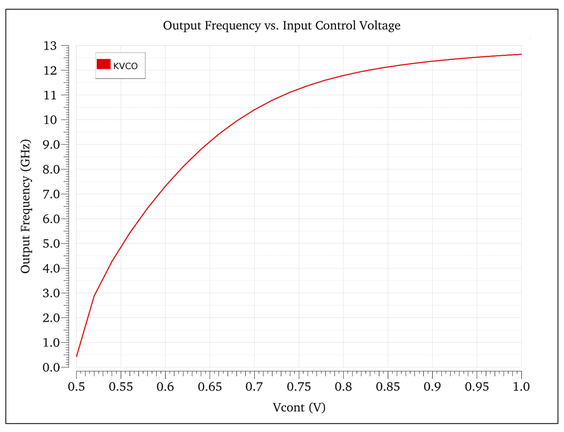
- At an input signal of 30 MHz, the PLL achieves a 7.680 GHz output while consuming about 69.98 µW.
- The entire design maintains an ultra-compact footprint, measuring only 6.5 × 37 µm².By employing a D-latch-based VCO, the architecture eliminates bulky LC resonators.
- Locking range spans the full 12.2 GHz VCO tuning range, supporting wideband coverage across multiple frequency bands.
- Overall, the results highlight a versatile, low-power PLL solution suitable for advanced 30 nm FD SOI technologies.



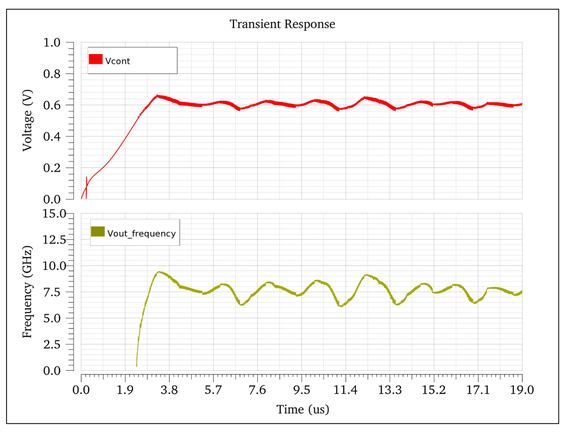
The schematic of the D-latch-based VCO and the D-latch circuits.



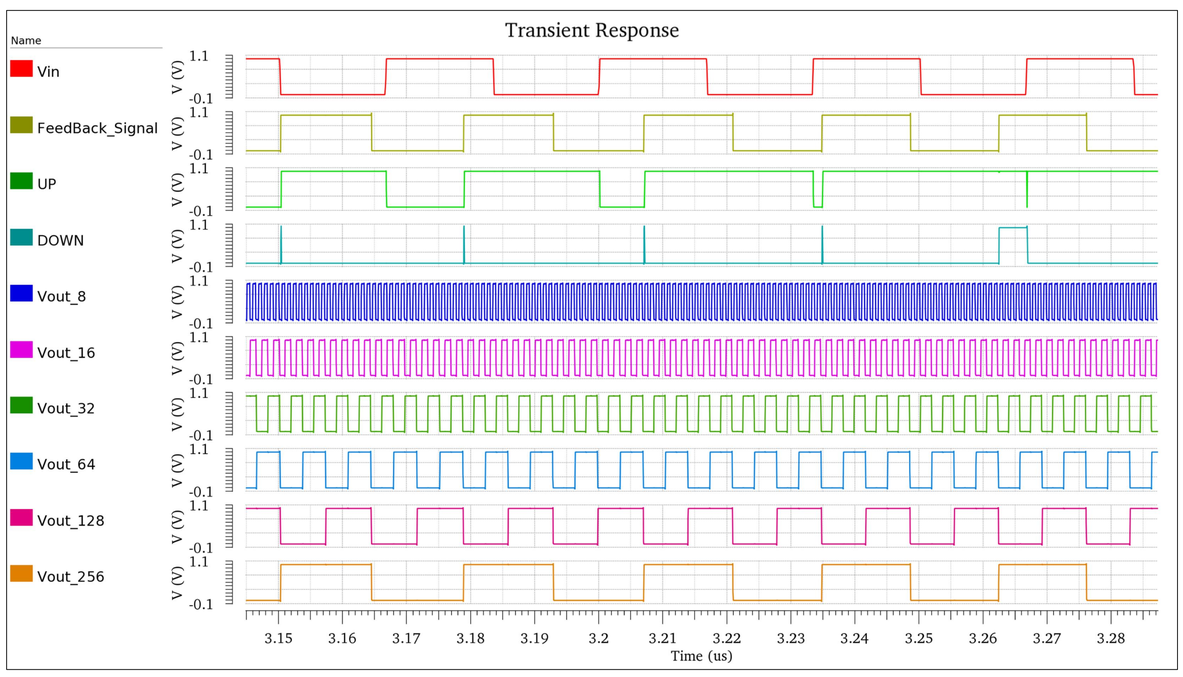
Core circuits of the PLL: (a) rising-edge detector, (b) phase-frequency detector, and (c) frequency divider using a negative-edge-triggered master-slave D-flip-flop.



The figure shows the D-latch VCO's output frequency vs. control voltage, illustrating a non-linear yet effective tuning profile.



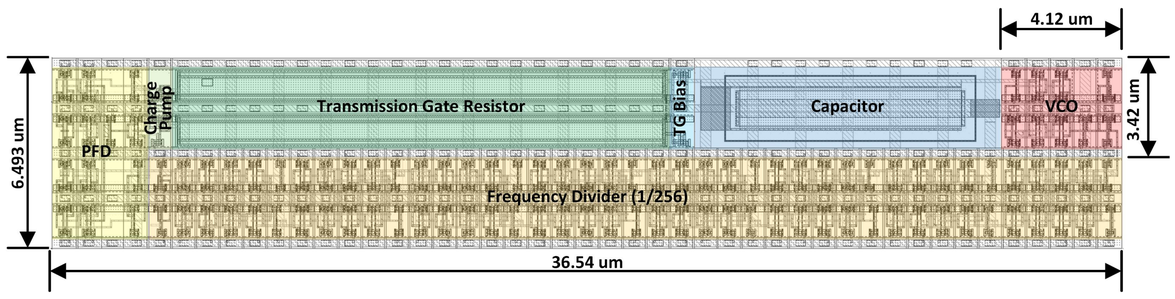
The figure shows simulation results of V_{cont} and V_{out} for a 30 MHz input. As V_{cont} adjusts, V_{out} effectively converges to 7.680 GHz.



Snapshot of the PLL near lock, showing the input, feedback, phase detector UP/DOWN signals, PLL output divided-by 8, 16, 32, 64, 128, and 256 signals.

Comparison With the State-Of-Art Table

Paper Title	Power Consumption (mW)	Area (um²)	Center Frequency (GHz)	Tuning Frequency Range (GHz)
A (0.75–1.13) mW and (2.4–5.2) ps RMS Jitter Integer-N-Based Dual-Loop PLL for Indoor and Outdoor Positioning in 28-nm FD-SOI CMOS Technology [TCAS II 2023]	1.27	346,000	5.44	0.56
A Noise Reconfigurable All-Digital Phase-Locked Loop Using a Switched Capacitor-Based Frequency-Locked Loop and a Noise Detector [JSSC 2018]	3.8	49,000	2.65	4.3
A Self-Calibrated Fractional-N PLL for WiFi 6 / 802.11ax in 28nm FDSOI CMOS [ESSCIRC 2019]	38	800,000	7.15	1.5
A 600µA 32 kHz input 960 MHz output CP-PLL with 530ps integrated jitter in 28nm FD-SOI process [ESSCIRC 2014]	0.972	150,000	0.56	0.81
This Work	0.070	240	6.53	12.2



The figure shows the integrated PLL design, indicating the detailed transistor-level layout.